

IN THE SPECIFICATION

Please replace the paragraph on page 1 under the heading "CROSS REFERENCE TO RELATED APPLICATIONS" with the following:

[0001] This patent application is a continuation of U.S. Patent Application Serial No. 10/119,571, filed on April 9, 2002, entitled "METHOD AND SYSTEM FOR REDUCING SHORT CHANNEL EFFECTS IN A MEMORY DEVICE BY REDUCTION OF DRAIN THERMAL CYCLING" that is, in turn, a divisional of co-pending U.S. Patent Application Serial No. 09/410,962 entitled "METHOD AND SYSTEM FOR REDUCING SHORT CHANNEL EFFECTS IN A MEMORY DEVICE BY REDUCTION OF DRAIN THERMAL CYCLING" filed on October 5, 1999, that is, in turn, related to U.S. Patent Application serial number _____ filed on _____ and entitled "METHOD AND SYSTEM FOR REDUCING SHORT CHANNEL EFFECTS IN A MEMORY DEVICE FORMED USING A SELF-ALIGNED SOURCE" and assigned to the assignee of the present invention. The present invention is also related to U.S. Patent Application serial number _____ filed on _____ and entitled "METHOD AND SYSTEM FOR REDUCING SHORT CHANNEL EFFECTS IN A MEMORY DEVICE" and assigned to the assignee of the present invention. The present invention is related to U.S. Patent Application serial number _____ filed on _____ and entitled "METHOD AND SYSTEM FOR REDUCING SHORT CHANNEL EFFECTS IN A MEMORY DEVICE THROUGH SELECTION OF A DOPANT" and assigned to the assignee of the present invention.

In the Claims

Please amend claims 1, 4, 5, 6, 9 and 19 and withdraw claims 27 and 28, as follows:

1 1. (Currently amended) A method for providing a semiconductor memory device
2 including a substrate and at least one field isolation region, the method comprising the steps of:
3 (a) providing a plurality of gate stacks above the substrate, each of the plurality of gate stacks
4 including a first edge and a second edge, each of the plurality of gate stacks crossing
5 the at least one field isolation region;
6 (b) providing a source implant adjacent to the first edge of each of the plurality of gate stacks;
7 (c) driving the source implant under the first edge of each of the plurality of gate stacks; and
8 (d) ~~masking the source implant; and~~
9 (e) ~~providing a drain implant after the masking step (c [[d]]),~~ the drain implant being
10 provided only in the substrate adjacent to the second edge of each of the plurality of
11 gate stacks.

1 2. (Previously cancelled)

1 3. (Previously presented) The method of claim 1 wherein the source implant providing
2 step (b) includes the step of:
3 (b1) providing a first source implant and a second source implant adjacent to the first edge of
4 each of the plurality of gate stacks; and
5 wherein the driving step (c) includes the step of:
6 (c1) driving the first source implant and the second source implant under the first edge of each
7 of the plurality of gate stacks.

1 4. (Currently amended) The method of claim 1 further comprising the step of:
2 (e [[f]]) providing a first spacer and a second spacer for each of the plurality of gate stacks,
3 the first spacer being disposed along the first edge of each of the plurality of gate
4 stacks, the second spacer being disposed along the second edge of each of the plurality
5 of gate stacks.

1 5. (Currently amended) The method of claim 4 further comprising the step of:
2 (f [[g]]) providing a self-aligned source etch.

1 6. (Currently amended) The method of claim 4 wherein the semiconductor memory
2 device further includes a periphery including a plurality of logic devices and wherein the spacer
3 providing step (e [[f]]) further includes the step of:
4 (e1 [[f1]]) providing the first spacer and the second spacer concurrently with a plurality of
5 spacers in the periphery of the semiconductor memory device.

1 7. (Original) The method of claim 1 wherein the drain implant is As.

1 8. (Original) The method of claim 5 wherein the second source implant is As.

1 9. (Currently amended) The method of claim 1 further comprising the step of:
2 (e [[f]]) providing a rapid thermal anneal after the drain implant has been provided.

1 10-16. (Previously cancelled)

1 17. (Previously presented) The method of claim 1 wherein the step of driving the source
2 implant under the first edge of each of the plurality of gate stacks comprises a thermal treatment.

1 18. (Previously presented) The method of claim 3 wherein the step of driving the first and
2 second source implants under the first edge of each of the plurality of gate stacks comprises a thermal
3 treatment.

1 19. (Currently amended) A method of fabricating a semiconductor memory, the method
2 comprising:

3 forming a stacked gate;

4 performing a source implant adjacent to a first edge of the stacked gate;

5 heat treating the semiconductor memory so that the source implant diffuses under the first
6 edge of the stacked gate;

7 performing a drain implant only adjacent to a second edge of the stacked gate; and

8 limiting the duration and temperature of subsequent heat treatments of the semiconductor
9 memory to reduce diffusion of the drain implant, ~~whereby~~ so that the source implant
10 extends further under the first edge of the stacked gate than the drain implant extends
11 under the second edge of the stacked gate.

1 20. (Previously presented) The method of claim 19 wherein performing the source
2 implant comprises performing a double diffused implant (DDI).

1 21. (Previously presented) The method of claim 19 wherein performing the source
2 implant comprises:
3 performing a double diffuse implant (DDI); and
4 performing a moderately doped drain implant (MDDI).

1 22. (Previously presented) The method of claim 19 wherein heat treating the
2 semiconductor memory comprises annealing the semiconductor memory at a temperature of between
3 about 800° and about 1000° Celsius for about 20 to about 200 minutes.

1 23. (Previously presented) The method of claim 22 wherein annealing the semiconductor
2 memory comprises heating the semiconductor memory in a furnace at about 900° Celsius for about
3 40 minutes.

1 24. (Previously presented) The method of claim 19 further comprising performing a rapid
2 thermal anneal after performing the drain implant.

1 25. (Previously presented) The method of claim 24 wherein the rapid thermal anneal
2 comprises heat treating the semiconductor memory in a furnace at a temperature of about 900° to
3 about 1000° Celsius for about 10 to about 30 seconds.

1 26. (Previously presented) The method of claim 19 further comprising forming first and
2 second spacers adjacent the first and second edges, respectively.

1 27. (Withdrawn) ~~The method of claim 26 wherein the source implant comprises a first~~
2 ~~source implant, the method further comprising performing a second source implant after forming the~~
3 ~~first and second spacers.~~

1 28. (Withdrawn) ~~The method of claim 27 wherein the second source implant is performed~~
2 ~~in conjunction with performing a connection implant.~~